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Control of Dynamic Voltage Restorer Using Novel Fast Two Vector Phase-Locked Loops Regulator

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ABSTRACT

A fast two-vector Phase-locked loops (PLL) control has been proposed to control the phase and frequency of the grid voltage using 48-pulse switching. The novel controller senses the phase shift of the grid voltage as a frequency deviation by the load and locked to the positive sequence. The controller was designed to track the grid voltage angle and kept the grid frequency within the satisfying rang at all the time. The PI- controller was proposed to obtain the desired performance of the PLL. The fast PLL phase shift of the grid voltage. The test results shows that the new design of controller can control the response of the positive sequence between -1.75p.u to 1.75p.u. With in-phase compensation. The proposed PLL controller has been simulated by using PSCAD/EMTD software package.

التحكم فى مستعيد الجهد الديناميكى باستحدات متجهين لتتبع الطورالحلقى المغلق المعدل

على عمر المثنانى [1] و على ليسيود [2] و جمال العكشى [1] و صالح ابوعزوم [1]

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الكلمات المفتاحية:
المتحكم الطوري الحلقي المغلق(PLL)
48نبضة لمستعيد الجهد الديناميكي
المتحكم بالاتجاهين
الجهد الهابط

الملخص

تتبع الاشارة بواسطة الطور الحلقي المغلق PLL باستخدام متجهين سريعين ثم اقتراحه للتحكم في الطور و التردد الموجب في جهد المصدر باستخدام 48 نبضة . العمل الجديد المقترح يتحكم في ازاحة الطور الذي يحدث في المصدر ويسبب في انحراف التردد الذي يوثر على الحمل ويعمل على اغلاق في التتابع الموجب.المتحكم صمم لتتبع ازاحة جهد المصدر ويتبت تردد المصدر خلال معدل مقبول كل الوقت . المتحكم التفاضلي التكاملي (PI) ثم القتراحةللحصمل على الاذاء المطلوب في الطور الحلقي المطلوب. متحكم الطور السريع يقوم بتصحيح زاوية الطور خلال الانخفاض المفاجئ (sag) .الكسب في المتحكم التفاضلي التكاملي (PI) يعتمد على ازاحة الطور في مصدر الجهد.النتائج توضح بان التصميم الجديد للمتحكم يستطيع التحكم في استجابة التتابع الموجب بين -1.75 pu و +1.75pu خلال تعويض الطور.المتحكم الطوري المغلق (PLL) ثمت محاكاتة باستخدام PSCAD.

1. Introduction

A dynamic voltage restorer (DVR) is a custom power device which is used to restore voltage during power quality disturbances such as voltage sags. DVR can maintain load voltage at the desired amplitude during voltage sag, by injecting a compensating voltage in series with the load. The ideal voltage restoration is to make the load voltage unchanged [1]. Our previous research [2] proposed two levels, 24-pulse to compensate the energy at 1p.u. The zero-crossing detection is used to estimate the phase angle of the grid voltage. The estimated angle tracks the actual angle and PLL locks it again in almost 160ms. This paper deals with a new kind of DVR is emphasizing on its control techniques to mitigate voltage sag for the non linear load. The control algorithm is based on the vector control approach and it

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consists of two control loops. The proposed algorithm incorporates both voltage and current controllers to improve the transient performance of the DVR. The response time of the proposed algorithm shows that it can rapidly restore system voltage. The phase angle of the grid voltage is exploited to calculate the reference of the injected voltage in the synchronous reference frame. An error in the phase-angle detection may lead to significant errors in the injected voltage and the load may be disturbed. Obtaining phase information has normally been done by the phase-locked loop PLL. In three-phase systems, the PLL has been proposed for DVR applications by transforming the three-phase voltage of the grid into the synchronous reference frame and the performance of the PLL is controlled by either a lead/lag filter or a PI-controller.

II. Dynamic Voltage Restorer (DVR)

A. Circuit Description

The basic configuration of DVR is that it consists of a control circuit and power circuit. Control circuit is used to derive the parameters such as magnitude, frequency and phase shift, of the control signal that has to be injected by the DVR. Based on the control signal, the injected voltage is generated by the switching control of the voltage source inverter (VSI) in the power circuit. Fig.1 shows the basic structure of the DVR along with the system. The voltage sag is mostly unbalanced and accompanied by phase angle. The DVR injects three-phase voltage in series by synchronizing the incoming supply voltage. The phase angle and magnitude of injected voltage are variable which result in variable real and reactive power that exchange between the DVR and distribution system. The injected voltage of the DVR can be written as

$$V_S = V_{DVR} + V_L \quad (1)$$

Where;

V_s is the source voltage during sags/swells condition

V_L is the desired load voltage magnitude

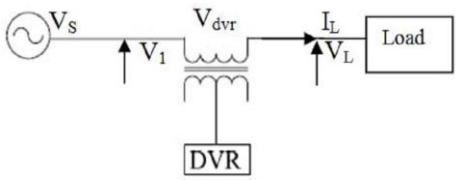


Fig.1: basic structure of the DVR

B. Zero-Crossing Detection

The zero-crossing in single phase system is used to estimate the phase angle of the grid voltage. The fast tracking performance is impossible and the dynamic performance of the loop is slow, because tacking one cycle to finish the processing. The accuracy of zero-crossing is influenced by harmonics. Despite the ease to write a zero-crossing detection algorithm but the dynamic performance of the loop is slow and a fast tracking performance is impossible [3].

C. Phase-Locked Loops (PLL)

The PLL as shown in Fig.2 consists of three main components a phase detection unit, low pass filter (LPF), and voltage controlled oscillator (VCO). The phase detection unit is generally implemented using a comparator. It is responsible for finding the difference between the phase angle of the input signal and the output signal. The output of the phase detection unit consists of two components. The first component is a function of the phase difference between the input signal and output signal and the second component is the double frequency ripple of the signal. Since the second component of the phase detection scheme output is not useful, it can be partially removed using the passive filter. The bandwidth of the passive filter should be small so that it can remove both the double frequency ripple as well as any unwanted noise. However, if the bandwidth is too small, then this will affect the dynamics of the system. Thus, choosing a proper filter bandwidth is an important for PLL design consideration. The output of the LPF then contains only the first component which is a function of the phase difference between the input and the output signals or the phase error. This error signal is then used to drive the voltage-controlled oscillator to generate an output signal. Ideally, the phase error should be zero, so that the phase angle of the output signal is identical to the phase angle of the input signal. The VCO produces a periodic output signal and the frequency of which changes depending on the applied control signal. When the phase error signal is zero the VCO generates an output signal at the centre of the frequency. However, when the phase error is not equal to zero, the VCO responds by changing its operating frequency. Essentially, the VCO is able to drive the phase error to zero by modifying its operating frequency.

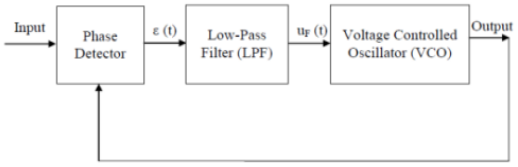


Fig. 2: General structure of the PLL scheme

D. Conventional Three-phase PLL

The PLL system is a feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal. As shown in Fig.3, the phase error is the difference between the actual phase angle ($\theta(K)$) and estimated phase angle ($\hat{\theta}(K)$) according to the following Eq. (2):

$$e(K) = \theta(K) - \hat{\theta}(K) \quad (2)$$

The closed loop Z-transfer function is the stability conditions of the PLL and can be obtained as:

$$G_{SPLL(z)} = \frac{\hat{\theta}(z)}{\theta(z)} = \frac{K_P T_S (z + K_I / K_P - 1)}{z^2 + (K_P T_s - 2)z + T_s(K_I - K_P) + 1} \quad (3)$$

Where T_s is the sampling time, and

$$Z = 1 - K_I / K_P \quad (4)$$

Where K_I and K_P are the integral and proportional gains of the PI-controller

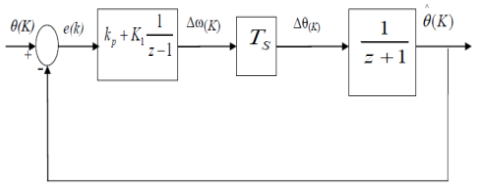


Fig. 3: Closed loop transfer function of the PLL

The loads are satisfactory if the source frequency deviation is kept within ± 1 Hz according to European Standard EN 50160, 2007. The change in the phase angle of the source is followed by the change in the source frequency with respect to time [3].

$$w(t) = d\theta / dt \quad (5)$$

The loads will not disturb by the change in the phase angle of the source, if $d\theta(t)/dt$ or $\Delta\theta(t)/\Delta t$ is kept within ±1 Hz.

Where $\Delta\theta$ is the Phase angle change

The change of the phase angle is by 2π radian (360^0).

$$\Delta\theta(t) / \Delta t = 2\pi \quad (6)$$

The required time to be obtained at steady state is the function of the $\Delta\theta$

$$\Delta t = \Delta\theta / 2\pi \quad (7)$$

There have been various works proposed to improve the performance of the single-phase PLL. The researcher [3] proposed the phase locked loop controller to obtain the phase and frequency information of the grid voltage. The PLL tracks the angle every eight cycles. Chung [4] introduced the PLL to control the single phase PWM inverter for constant voltage and constant frequency.

Ramasamy and Kasuni [5, 6] reported that the method to track the phase angle is not accurate and not suitable for fast synchronization. Since the single-phase PLL has no internal harmonic cancellation and generates a double frequency ripple. Ref [6] present a slow PLL to allow a smoother operation for sudden phase shifts at every cycle. The PLL compensator utilizes a phase difference of 90^0 between the capacitor voltage and current, which is singular to the *dq* variable in the three-phase system. The proportional integral (PI) controller is used in single-phase PWM inverter to eliminate the steady-state error [4].

III. PLL Modelling

The PLL tracks and controls the frequency variation of three phase signals in which the grid voltage sampling is assumed as,

$$u_1 = \sqrt{2}U\cos(\theta) \quad (8)$$

$$u_2 = \sqrt{2}U\cos(\theta - \frac{2\pi}{3}) \quad (9)$$

$$u_3 = \sqrt{2}U\cos(\theta + \frac{2\pi}{3}) \quad (10)$$

where U is the phase to ground RMS grid voltage. The $\alpha\beta$components of the grid voltage are calculated as

$$\begin{pmatrix} u_{g\alpha} \\ u_{g\beta} \end{pmatrix} \frac{2}{3} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\sqrt{\frac{3}{2}} & \sqrt{\frac{3}{2}} \end{pmatrix} \begin{pmatrix} u_{g1} \\ u_{g2} \\ u_{g3} \end{pmatrix} \quad (11)$$

After normalization to $\|ug^{\alpha\beta}\|$ the $\alpha\beta$ components of the grid voltage become:

$$\begin{pmatrix} u_{g\alpha} \\ u_{g\beta} \end{pmatrix} = \begin{pmatrix} \cos(\theta) \\ -\sin(\theta) \end{pmatrix} \quad (12)$$

The positive sequence is extracted to obtain ugαp and $ug\beta p$
The *dqp*-components of the grid voltage are calculated as:

$$\begin{pmatrix} u_{gdp} \\ u_{gqp} \end{pmatrix} = \begin{pmatrix} \cos\left(\hat{\theta}\right) & \sin\left(\hat{\theta}\right) \\ -\sin\left(\hat{\theta}\right) & \cos\left(\hat{\theta}\right) \end{pmatrix} \begin{pmatrix} u_{g\alpha p} \\ u_{g\beta p} \end{pmatrix} \quad (13)$$

Where $\hat{\theta}$ is the estimated angle by the PLL. It is worth to mention that as the synchronizations is made with respect to a virtual flux vector, $-\frac{\pi}{2}$ is added to the estimated angle. After algebraic manipulation, the *dqp*-components of the grid voltage can be derived as:

$$\begin{pmatrix} u_{gdp} \\ u_{gqp} \end{pmatrix} = \begin{pmatrix} -\sin\left(\theta - \hat{\theta}\right) \\ \cos\left(\theta - \hat{\theta}\right) \end{pmatrix} \quad (14)$$

When the difference $\theta - \hat{\theta}$ approaches zero and the *dqp*-component approaches to $u_{gdp} \cong 0$ and $u_{gqp} \cong 1$

Eq. (12) represents a nonlinear relation where the *d*-component of the grid voltage u_{gdp} is a function of the sine of the difference between the actual and estimated phase angles.

IV. PI Mode Controller

The conventional PI controller is its effectiveness in the control of steady state error of a control system and also its easy implementation. However, one disadvantage of this conventional compensator is its inability to improve the transient response of the system [7]. Most of PI controllers can be used in cascade loop control

due to the *dq* components of the injected voltage and current. The conventional PI controller as shown in Fig.4 has the form:

$$U(t) = K_P \varepsilon(t) + K_I \int_T \varepsilon(t) d(t) \quad (15)$$

Where *U* is the control output which is fed to the pulse width modulator (PWM) as signal generator. K_P and K_I are the proportional and integral gains, respectively. These gains can be tuned depend on the system parameters in order to minimize the ε (the difference between the injected voltage and the reference voltage).

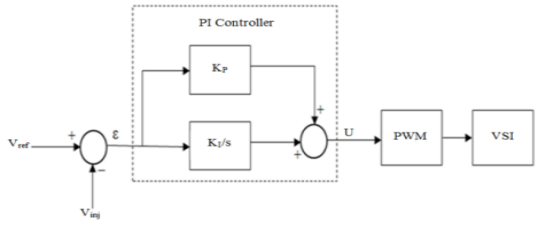


Fig. 4: Control of the injected voltage using conventional PI controller

V. Development of DVR Configuration

DVR can be considered as the device that injects a voltage waveform to the distribution line. The DVR injects only the difference between the pre-sag and the sagged voltage during the sagged period. The DVR is VSI that converts the DC voltage supplied by the energy source capacitor (ESC) into an AC voltage. ESC is used to supply the real power requirements for the compensation during voltage sag. The control technique is to detect and compensate for three phase voltage sag. The passive filter is used to convert the PWM inverted pulse waveform into a sinusoidal waveform and reduce the harmonic contents. The basic function of the injection transformer is to increase the voltage supplied by the filtered DVR output to the desired level and isolate the DVR circuit from the distribution network. The rating of the injection transformer is an important factor when deciding the DVR performance. A simplified test distribution system including DVR is implemented using the PSCAD/EMTDC simulations for evaluating the voltage sag mitigation capability of the DVR as shown in Fig.5. The test system comprises an 11 kV transmission line, feeding into the step down transformer. The DVR is placed in series with 0.415 kV distribution systems along with the 0.02MVA load.

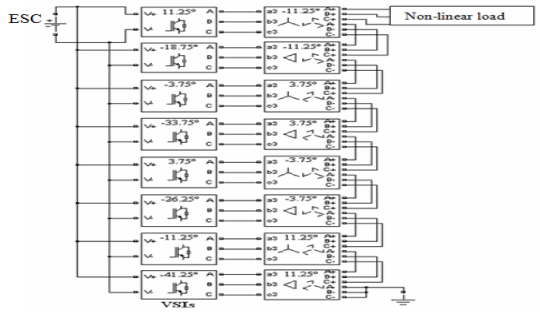


Fig. 5: PSCAD Simulation model for 48-pulse switching

The DVR was activated and injected the voltage to the distribution system when the sag, swell and interruption occurred. The magnitude and the phase angle of the supply voltage can be changed and it was denoted by V_{sag}. The controller can control the magnitude and angle independently. If the voltage sag is fully compensated by the DVR, the load voltage during the voltage sag will be $V_{pre\text{-}sag}$. The PWM controls the active and reactive power fed from the ESC link can produce voltage to the system.

A. Control of DVR

Fast two continuous PLL vector controllers are cascade controllers using two vector control loops *i* and *u* that track the reference of the injected voltage as well as to compensate for the voltage drop across the LC-filter as shown in Fig.6. The reference of the injected voltage is calculated by subtracting the measured source voltage at PCC from the reference of the load voltage;

$$\overset{*}{u}_{inj} = \overset{*}{u}_c = \overset{*}{V}_L - V_1 \quad (16)$$

Where V_1 and V_L^* are the source voltage at PCC and the reference of the load voltage, respectively. It is important to consider that the effect of LC filter mounted at the output of the inverter, as shown in Fig.6. The filter can reduce the unwanted injection capability of the device and introduce a phase shift in the injected voltage.

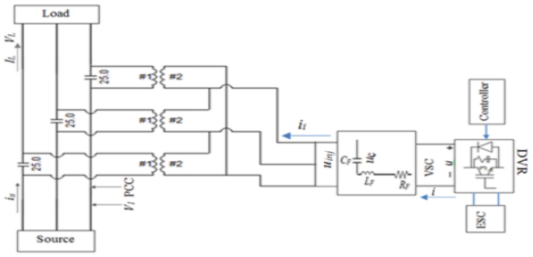


Fig. 6: Three-line diagram of DVR including inverter, LC filter and transformers

B. Two Continuous PLL Vector Control Modelling

The proposed control strategy as shown in Fig.7 is used in the DVR for injecting a small active power during voltage sag, maintains constant voltage magnitude at the point under the system sag. Then it shifts the inverter into the converter mode to charge the ESC system during normal state in the absence of voltage sag and force the load voltage to be in-phase with the source voltage during the sag.

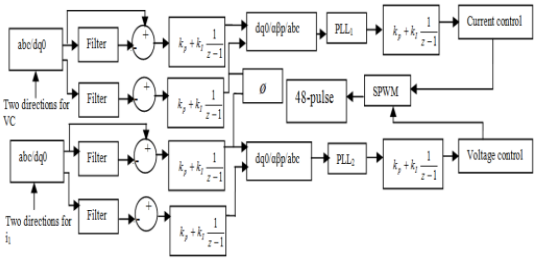


Fig. 7: Block diagram of the two continuous PLL vector

The PLL is proposed to keep the load voltage synchronized continuously. This component is a 3-phase, PLL controlled phase locked loop, which generates a ramp signal theta that varies between 0 and 360^0, synchronized or locked in phase, to the input voltage. The phase error is passed as an output variable after conversion to degrees. The frequency of the input is computed and returned as internal output parameters called tracked frequency.

The PLL with a PI controller have been proposed for the DVR to satisfy the frequency requirement of the load. This is important to control the energy flow between the DVR and the source. The gains of the PI controller are selected properly to make PLL behaves as low pass filter, thus the harmonic in the grid voltage may not affect the performance of the PLL. In the case of voltage sags in the source voltage, the PLL and the DVR perform satisfactorily such that the load voltage magnitude is restored to the pre-sag value and the phase angle of the load voltage tracks the phase angle of the source voltage without experiencing a sudden phase angle shift. As shown in Fig.7, the proportional gain and the integral gain of the PI are 50 and 500 respectively. The main parts of the controller are the three-phase abc to dq0 transformation, filter, PI controller and PLL. The PI controller is used for interpolated firing pulses and the PLL for tracking the system. The *dq0* is connected between the PLL and PI controller to minimize the grid voltage error and to extract the reference voltage for the DVR. The fast PLL two continuous vector control algorithm is implemented in the dq-frame and incorporates both current and voltage controller with an inner current control loop and outer voltage control. The current and voltage control are based on two continuous vector controls. When the sag is detected, the PLL locks the pre-sag voltages, thus the difference between the reference voltage load and the source voltage generate the injected voltage from the DVR. The Park's *dqo* transformation formula is shown as follows:

$$[V_d V_q V_o] = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta - \frac{4\pi}{3}) \\ \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \cos(\theta - \frac{4\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (17)$$

Equation (17) defines the transformation from abc dynamic frame to dqo stationary frame. Phase a is aligned to the *d* axis that is in quadrature with the *q*-axis. The θ is the angle between phase a to the *d*-axis. For simplicity, zero sequence components should be ignored.

$$Vo = \frac{1}{3}(Va + Vb + Vc) = 0 \quad (18)$$

$$Vd = \frac{2}{3}\left[Va\sin wt + Vb\sin\left(wt - \frac{2\pi}{3}\right) + Vc\sin\left(wt + \frac{2\pi}{3}\right)\right] \quad (19)$$

$$Vq = \frac{2}{3}\left[Va\cos wt + Vb\cos\left(wt - \frac{2\pi}{3}\right) + Vc\cos\left(wt + \frac{2}{3}\right)\right] \quad (20)$$

In This method the reference voltage for the DVR is the sine waveform PWM. This is generated by comparing the pre-sag voltage with the actual voltage. The dynamic performance of the DVR may be improved by controlling both the inductor current and capacitor voltage of the LC-filter. Fast two continuous PLL vector controllers are the proportional controller type. They are proposed to track the reference of the injected voltage and also to compensate for the voltage loop across the LC-filter which is connected at the output of the DVR. The injected voltage is derived as:

$$V_{dvr} = V_L - V_1 \quad (21)$$

Where V_L and $V_1$are the load voltage and voltage at PCC, respectively.

Transform from positive *dqp*-frame to αβp-frame to get the positive sequence component of the grid voltage u_{gdp} and u_{gqp}. The *d*-component of *ugdp* is the input to the proportional-plus-integral (PI) controller and PLL to calculate the change in the angular frequency of the grid voltage Δw.

$$\Delta w = (K_P + K_I/(Z-1))u_{gdp} \quad (22)$$

Where K_P and K_I are the proportional and integral gains of the PI–controller.

C. Configuration of Two Continuous PLL Vector Controllers

To derive the system equation of the Fig. 6, the involved state variable include the fault supply voltage (V_1) at PCC, load voltage (V_L), series injected voltage (u_{inj}), LC filter capacitor voltage(u_c), DVR output voltage (u), current (*i*), series injected current(i_i) and ESC. The reference of the compensator injected voltage (u_{inj}) is obtained by subtracting the load voltage (V_L) from the nominal voltage (V_1), and then performing line to phase voltage transformation. The series injected voltage has a relation to the capacitor voltage (u_c) based on the turns of the voltage matching transformers. The converter output voltage (*u*) is obtained in terms of the modulation index (*m*) and the sensed the dc-bus capacitor voltage V_{dc} as:

$$V_m = m.V_{dc}/2 \quad (23)$$

By applying Kirchhoff's current and voltage laws, the following system equation are

Obtained,

$$C_f \frac{d}{dt}(u_c) = i - i_i \quad (24)$$

$$L_f \frac{d}{dt}(i_m) = \frac{1}{2} m.V_{dc} - V_C \quad (25)$$

To derive the controller, the LC filter should be modelled in the stationary abc coordinates into synchronously rotating *d-q*. This allows the design of controllers to use DC dynamic model in balanced three-phase AC systems. As shown in Fig 6, the state variable have null zero sequence components. Thus, *d, q* transformation of the system Eqs in (24)and (25) yields,

$$\frac{d}{dt}(u_C)_{dq} = \omega\Phi(u_C)_{dq} + \frac{1}{C_f}(i_m)_{dq} - \frac{1}{C_f}(i_i)_{dq} \quad (26)$$

$$\frac{d}{dt}(i)_{dq} = \omega\Phi(i)_{dq} + \frac{V_{dc}}{2L_f}(m)_{dq} - \frac{1}{L_f}(u_c)_{dq} \quad (27)$$

$$\Phi = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$$

Where, and ω represents the angular frequency of the 50 Hz AC system

The controller equation of the reference voltage and current can be derived as:

$$u^{*dq} = u_c^{*dq} + R_F i^{*dq} \pm j\frac{\omega L_F}{2}\left\{i^{*dq} + i^{dq}\right\} + K_P\left\{i^{*dq} - i^{dq}\right\} \quad (28)$$

$$i^{*dq} = i_s^{dq} \pm j\frac{\omega C_F}{2}\left\{u_c^{*dq} + u_c^{dq}\right\} + K_u\left\{u_c^{*dq} - u_c^{dq}\right\} \quad (29)$$

Where, u^{*dq} and i^{*dq} are the required reference voltage and currents to track the reference of the injected voltage and *j* is the phase shift between *d* and *q* components. ω is the angular frequency of the grid voltage and C_F, R_F and L_F are the parameters of the filter of the DVR. K_u and K_P are the dead-beat and proportional gains of the filter and derived as follows:

$$K_u = \frac{C_F}{T_s}, \quad K_P = \left(\frac{L_F}{T_S} + \frac{R_F}{2}\right) \quad (30)$$

Where T_S is the sampling time.

The integral gain is

$$K_i = \frac{K_P T_S}{T_i} \quad (31)$$

Where T_s and T_i are the sampling time and integration time respectively. The integral time should be greater than the sampling time to keep the system stable. The current of the VSC is higher than the source current. This implies that if the load/source current is measured on the high voltage side, the source current i_s in Eq.(29) should be multiplied by the turns ratio of the injection transformer. The voltage drop due to the leakage impedance of the injection transformer should be calculated and added to the reference voltage of the VSC as in Eq.(32), where R_T and L_T are the resistance and leakage inductance of the transformer.

$$u^{*dq} = u_c^{*dq} + R_T i_s^{*dq} \pm j\omega L_T i_s^{*dq} + R_F i^{*dq} \pm j\frac{\omega L_F}{2}\left\{i^{*dq} + i^{dq}\right\} + K_P\left\{i^{*dq} - i^{dq}\right\} \quad (32)$$

PLL_1 generates a sinusoidal signal with controllable magnitude and frequency, whereas PLL_2 generates a triangular waveform. The triangular waveform has a switching frequency, which is 30 times the fundamental frequency of 50 Hz, i.e. 1500 Hz. This frequency is used for switching the DVR inverter switches. The 50 Hz reference sine wave is then compared with the triangular waveform using the SPWM technique to generate the switching pulses. A PSCAD model has been designed to test the proposed controller and the results are shown in next section.

VI. Simulation Results

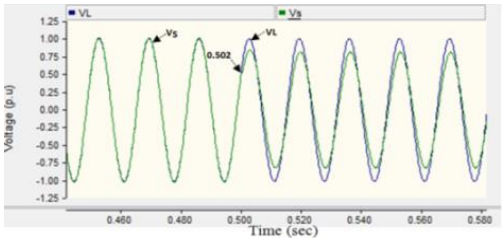
A PSCAD/EMTDC model has been built to simulate the system displayed in Fig.5 where DVR operated at 11kV line. To obtain an 11kV line, a step-down transformer 11/0.4 kV are installed.

A. Voltage Sag Mitigation Using DVR

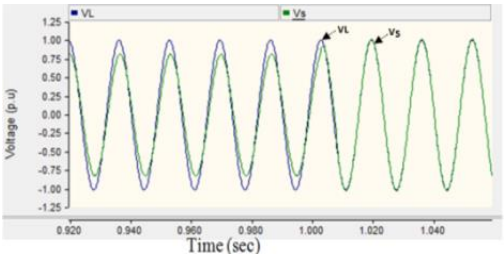
The DVR is designed to compensate for voltage sag at the load side and reduce the harmonics and transient. As shown in Fig.5, the fault is chosen as a balanced three-phase fault with fault resistance and inductance of 3Ω and 0.01 H, respectively. The controller is designed to compensate the system during the sag even with nonlinear load without harmonic and delay.

B. Performance of PI Controller

The PI controller with PLL has been proposed for the DVR to control the angle between the load and the source at the start of sag and the end of sag. The voltage of one phase of the load voltage and the source voltage are shown in Fig. 8. In case of no sag condition, the load voltage is equal to the source voltage. During the sag, the source voltage decrease and the load voltage in this design is kept at the same level as in normal operation. It can be noted from Fig.8a and 8b, the phase of the load and the source are the same at the beginning and end of the sag while the load voltage is kept constant during the sag. Thus, the load voltage is protected against sudden phase jumps associated with voltage sag in the source. The DVR can sense the sag in point 0.502p.u at the time near the 0.5sec when the sag starts. Also the figures show that the start and the end of compensation voltage are in phase with the source voltage and load voltage, respectively. These figures displayed that the compensation is within 2 ms without any harmonic distortion and phase shift during the sag. The design of new controller can improve the in-phase compensation technique during the nonlinear load when compared to the conventional controller.



(a)



(b)

Fig.8: Load voltage (VL), source voltage (VS) during sag (between 0.5 to1.0 seconds) and compensation (a) at the beginning. (b) at the end of simulation.

C. Performance of PLL

The PLL is developed to track the angle and frequency of the supply in every half cycle compared to the conventional design. Any change from the normal operation condition can easily be detected as shown in Fig.9. From the figure, it can be seen that the supply voltage and the angle operate exactly at the zero crossing point. The controller has been designed to detect and compensate the PQ disturbances in short time. The PLL, PI and *dq* are modeled to improve the system. The voltage sag is detected by comparing the pre-sag voltage with the actual voltage to generate the reference sin wave of the PWM.

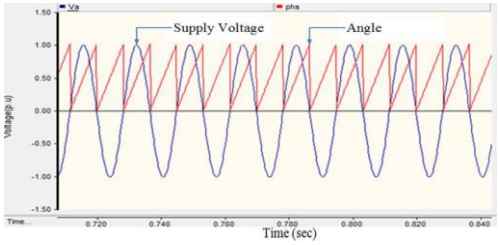


Fig. 9: Phase angle detection

The response of the positive sequence of the capacitor $(uc)_{dqp}$ is depicted in Fig. 10. Before the sag, $u_c dqp$ and $u_c{*}dqp$ are zero. When the sag starts, $u_c{*}dqp$ jumps instantaneously to -1.75 p.u. due to phase shift of the grid voltage. Then, $u_c{*}dqp$ rises back to zero and $u_c dqp$ follows $u_c{*}dqp$. When the sag is ended, $u_c{*}dqp$ jumps instantaneously to 1.75 p.u. The estimated angle gradually tracks the actual angle and PLL locks again after almost 0.5 sec from the sag start. The phase angle shift of 25^0 is obtained due to the simulated sag. The *dq* has the characteristic such as fast response without voltage oscillation in the transient state and low error in the steady state. The fast response in transient state guarantees faster action against the voltage sag and the low error in the steady state guarantees enough voltage compensation against voltage sag.

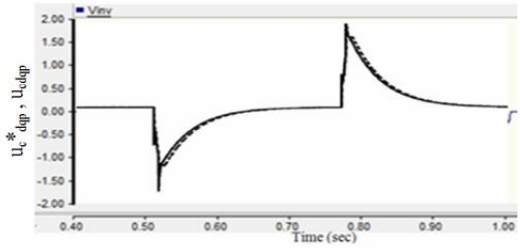


Fig.10: Response of positive sequence of capacitor reference voltage (solid) and actual voltage (dashed)

The controller was able to control the capacitor voltage (u_c) and analysis the steady–state response, thus can kept the load voltage constant without phase shift. The *d*-and *q*-voltage are shown in Fig.11.The *q*-voltage of the grid decrease, the *d*-voltage of the capacitor voltage increase to keep the load voltage constant.

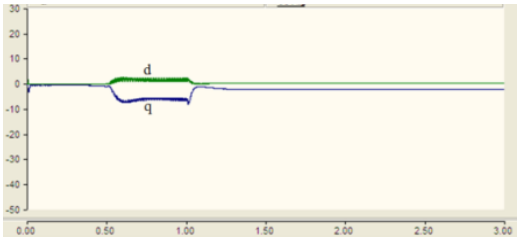


Fig.11: Response of the d-voltage of the capacitor and the q-voltage of the source

Conclusions

The DVR has been developed as a 48-pulse inverter connected in parallel to increase the efficiency of the DVR. The design of the controller has been developed to inject the required voltage in order to force the load voltage to be in-phase with source voltage. The newcontroller can restore the load voltage to 0.99 p.u with nonlinear load. The fast PLL with a PI was designed to track the phase change during a fault in every half cycle and behaved as a low pass filter to mitigate the harmonic in the source and synchronous *dq*-frame. The simulation results show that the DVR compensated the voltage sag quickly and provided excellent voltage regulation without harmonic distortion. The PLL has been done to control the frequency deviation for the most of loads. The positive sequence of the voltage was extracted and PLL is locked. The phase angle of the load voltage tracks the phase angle of the source voltage without a phase shift. The proposed control strategy has proofed satisfactory operation, both in terms of response time and smoothness of the injected voltage compensation. The response time of the DVR with the proposed control strategy was less than that proposed in the conventional design. Better efficiency was achieved with the new proposed control strategies. The injecting capability of the DVR with the two vector control algorithms has been tested through a PSCAD/EMTDC simulation model. A voltage sag of the rated grid voltage was originated and the DVR with the two vector control was capable of maintaining the load voltage constant with fast response of 2 ms.

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