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Structural, optical and electrical properties of SnSe4 for phase change memory

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Abstract A fabrication progress of phase change memory (PCM) has been reviewed in this paper. Simple structure contents from (Gl, Al, SnSe4, Al) were used. Where both Glass and Phase change material SnSe4 prepared individually, and deposited by using evaporation. In Crystallization kinetics SnSe4 has been investigated for phase change memory applications by using annealing. The SnSe4 shows that a low threshold voltage and current can cause transitions from amorphous to crystalline phase, where that confermed by I-V measurements. Furthermore, the crystallization temperature of the SnSe4 alloys is around $350 \,^{\circ}\text{C}$, where this tempreture acquired due to the phase transition, which has been confirmed by X-R Diffraction results. In addition, band gap has been calculated with UV test and showed that SnSe4 alloy is semiconductor, where the bad gap was 1.65 ev. The Dc measurement illustrates that PCM can transiate from amorphous to crystalline at threshold voltage of $3.2 \,\text{v}$ with high resistivity of 0.98 Mega ohm, where the crystalline resistivity is 19.3 K ohm. Morover; the pulse test has been investigated to show that the transition process happened with a pulse magnitude 1.6 v and time 33 Micro second.

Keywords: Annealing, amorphous, band gap, Crystallization, I-V measurements, X-R Diffraction.

الخصائص الهيلكية والبصرية والكهربائية SnSe4 ذاكرة تحويل الطور *خالدعبدالله الجليدي¹ و شاسي جيرهام بول² ¹ قسم الهندسة الالكترونية- كلية الهندسة- جامعة ديمونت فورت، بريطانيا ² قسم الهندسة النانو – كلية الهندسة – جامعة ديمونت فورت، بريطانيا Khalidaljledi@gmail.com:

الملخص في هذه الورقة تم استعراض طريقة تصميم ذاكرة التغير في الطور (PCM) باستخدام محتويات بنية بسيطة من (GI,AI,SnSe4,Al) حيث تم اعداد كلا من الزجاج ومادة تغيير الطور SnSe4 بشكل مستقل واودعت باستخدام التبخر،حركية التبلورللمادة SnSe4 قد ثم التحقق منها باستخدام التسخين الحرارة العالية . المادة SnSe4 تظهر انه في الجهد المنخفض والتيار القليل يسبب انتقال من مرحلة الغير متبلور الي المرحلة المتبلورة حيث يظهر في اختبار IV ، واضافة الى ذلك فأن حرارة التبلور للمادة المتحولة الطور هيا 350 درجة مئوية المكتسبة بسبب المرحلة الانتقالية ،والتي تم تاكيدها باستخدام اختبار نتائج الانعراج XR ، بالاضافة الى ذلك ، ثم حساب قيمة الفجوة باستخدام اختبار UV والنتائج اظهرت ان سبيكة SnSe4 شبه موصله ، حيث كانت قيمة الفجوة 1.65 va . وتوضح قياسات DC ان معدة PCM يمكن ان تنتقل من غير المتبلورة الى بلورية عند 3.2 فولت مع مقاومة عالية 0.98 ميقا اوم ، وحيث المقاومة البلورية هو 13.9 يمكن ان تنتقل من غير المتبلورة الى بلورية عند 3.2 فولت مع مقاومة عالية عادي 0.98 ميقا المقاومة البلورية هو 13.9 يمكن ان تنتقل من غير المتبلورة الى بلورية عند 3.2 فولت مع مقاومة عالية عالية الفورة 1.65 ميقا المقاومة البلورية هو 13.9 يمكن ان تنتقل من غير المتبلورة الى بلورية عند 3.2 فولت مع مقاومة الفجوة 1.65 به منقل أوم ، وحيث المقاومة البلورية هو 13.9 يمكن ان تنتقل من غير المتبلورة الى بلورية عند 3.2 فولت مع مقاومة النتائج انه عملية الانتقال تحدث عند 1.6 فولت وزمن 33 ميكرو ثانية.

الكلمات المفتاحية: (اختبار الحرارة العالية، الجسم الغير متبلور، الفجوة، الجسم المتبلور، اختبار الاشعة السينية).

Introduction

Similarly as with numerous current innovations, the degree that the non-volatile memory (NVM) invaded people's everyday lives is genuinely momentous. NVM which known as Flash memory is almost all over the place around. Together NAND and NOR flash started modestly enough, like overlooked side activities of a Toshiba DRAM engineer named Fujio Masuoka [1]. However, according to his rights in 1980 and 1987, correspondingly [1], the Flash had developed in under three decades to turn for the semiconductor industry into about \$20 billion dollar for every year [2,3]. The development of this business sector has been made conceivable through enormous builds in functionality of the system (e.g., farther G Bytes), which could be conveyed in the bundle with similar size. Both these changes are the main

thrust for and the side effect of the persistent differs to more diminutive gadget measurements known as Moore's Law [4].

A historical backdrop of the industry of solid-state memory, and generally of the semiconductor manufacturing, has been overwhelmed with this idea: greater concentrations at comparative expense produces more usefulness, and subsequently additional applications that then goad speculation on behalf of extra innovative work required to actualize the "next size smaller" gadget. All through that far- reaching history, from the later past estimation, it has turned out to be incredibly dependable for anticipating closefuture advancements. Therefore a memory items which shall be inherent the following a few years will have been extensive prediction [5]. Elsewhere

the nearby- future, not with standing, whilst the arranged gadget dimensions might be outlined out, without precedent for some years, it is not obvious precisely in what way attainable these objectives may be. That vulnerability is available in numerous parcels of the industry of semiconductor,[6] essentially because of expanding essentialness of gadget-to-gadget varieties, and to the basic reliance on proceeded with lithographic development. New designing systems shall in all likelihood be required to supplant the 193 nm involvement and "double patterning" methods now will be utilized to actualize the 32 nm and also 22 nm nodes [7]. Additionally, like these concerns normal for the bigger semiconductor manufacturing, nonetheless, the flash manufacturing confronts extra instabilities particular to its technology[8].

Experiment procedure

The main idea of this paper is to fabricate PCM using cheap alloys and simple procedure. For that reason many researches have been done and as a result SnSe4 has been found as the cheaper alloys that can be used with simple structure.

The PCM cell is contenting from 4 parts, from bottom to top, substrate is for Glass (Gl), and this works as heater terminal, then the bottom electrode which is from Aluminum (Al), after that Phase Change Material (SnSe4), Selenium and Tin, finally, the top electrode that is made from Aluminum. The figure (1) illustrates the procedures of the PCM fabrication. It can be done in the following steps:

- 1. Preparing wafer Substrate Glass (Gl).
- Deposit bottom electrode (Aluminium Al).
- Deposit bot
 Preparing Phase Change Material film (SnSe4).
- 4. Deposit SnSe4 over bottom electrode.
- 5. Annealing.
- 6. Deposit top electrode (Al).



Figure (1): preparing the sample

Preparing Phase Change Material film (SnSe4)

Phase change material (SnSe4) has been prepared by deciding which thickness should be used for each material in this experiment. The thickness that used for (SnSe4) is 150 nm. Where it divided into layers with different thickness for each material, namely, Sn and Se. thickness for Selenium is measured by calculating the Tin thickness by using the some equations find the

value of Density /Volume/Mass and Numbers of Atoms)

The General idea that the thickness for Selenium and Tin has been calculated by determining the number of atoms and from that ratio the thickness of Tin will be calculated.

After this calculation ratio cheked and it is found to be equal to 4 (SnSe4). Then, to the thickness of Se can be calculated. In this experiment there are two different thicknesses for (SnSe4) materials have been fabricated.

As a result the thickness of PCM used, SnSe4, is 160nm. Which consists of selenium with 120 nm thickness and Tin with thickness of 29.45nm.

Deposition system

The SnSe4 thin films were deposited in Edwards 306 sputtering/evaporation system using the evaporation technique. Before every deposition, the vacuum chamber is evacuated to (3-4) x10-5 mbar using the diffusion pump backed by a roughing pump. The boat used to evaporate the sample consisted of molybdenum (Mo) has very high melting temperature (Tm= 2623C°). This molybdenum boat was connected between the two copper electrodes. The electrodes were connected to a high current, low voltage source to pass high current through the boat, which was containing the ground samples of the alloy. By passing high current, the material in the boat turned into molten state and vapours were formed. These vapours were transported to the substrate by convectional currents and the films were deposited

On the rotating substrates and after deposition, the slides containing the deposited film were kept in the deposition chamber in the dark medium for 2 hours, so that the films attain thermodynamic equilibrium. The films were then removed from the chamber and stored in the slide holder

First layer has been deposited is Aluminium with Glass wafer the figure(2) below shows the Aluminium with Glass wafer after deposition, where the Aluminium works as bottom electrode .



Figure(2): shows (Glass and Aluminium wafer) The second layer that has been deposited is phase change material (SnSe4 with thickness of 150 nm) and this material consists of (120 nm Sn) and (29.45nm Se).

Annealing Sample

After deposited the two materials with Glass and Aluminium, this sample has been annealed at temperature of 350 C° to mix Sn and Se together and also to be sure that the material will change to crystalline. The table (1) below shows the steps of annealing.

Table (1): Shows	annealing	steps
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Temperature	Applied voltages
From (0-150) Co	170 v
From (150-200) Co	160v
From (200-250) Co	190v
From (250-300) Co	170v
From (300-350 Co)	160v
350 Co	Between (160-190)v

The last wafer has been deposited over the annealing sample is the Aluminium wafer (Al), with thickness of 100 nm. Where this wafer is working as Top electrode. The figure (3) shows the final shape of PCM cell.



Figure (3): Final shape of PCM with 150 SnSe4 thin film

Tests and Results

1.Optical Measurement

To obtain optical constants, Agilent VEE software was used to fit the experimental data to the simulated data and the results presented in the figure (4) below.





From the previous graph, to calculate the value of band gap equation (1) are used, where this equation created by Bardeen,

 $(k * hv)^{\frac{2}{n}} = A(hv-E_g - , +E_p) \dots (1)$

Where A is edge width parameter, E_p is photon energy, v is the frequency, and h the Planck's constant, while n carries the value of either 1 or 4. $E_p = 0$ for direct transition as there are no photons involved. The graph below in figure (5) shows the plot of $(k * hv)^{\frac{1}{2}}$ n as a function of hv for the film which n=4.

As a result, the band gap has been calculated and simulated by using Agilent software. As a consequence, the result is showing that the direct band gap is approximately 1.65 ev. Which means that the SnSe4 alloy is semiconductor. Moreover, less energy needed to push the electrons into conduction band from the Fermi level, figure (5) illustrate the method of calculation.



Figure (5): Shows relation between $(k * hv)^{\overline{2}}$ and photon energy of as deposited 160 nm SnSe4.

2.The X-Ray diffraction Results

The XRD has been done to SnSe4 film where two samples are used, before annealing and after annealing. The figure (6) shows the result for these two samples. As a result, the SnSe4 thin films show that they have an orthorhombic crystal structure.

The thin film shows that amorphous phase with extremely low degree. The annealing film also shows crystalline peaks at different angels at ((2θ b 15°)(2θ b 32°)(2θ b 43°)(2θ b 48°)).



Figure (6): X-ray diffraction patterns of 150nm as deposited and annealed (350 °C) SnSe4 thin films

3.Electrical Measurement DC test (Voltage switching) Results

This test has been done for many devices. The most perfect result is shown in device number (1d). When the applied voltage above 3.2v the resistance will be high, which is an amorphous phase, where the value of resistance at threshold volt is:

$$R = \frac{V}{I} = \frac{3.1}{3.26 * 10^{-6}} = 0.95 Mega Ohm$$

The figure (7) shows that, at the threshold volt (3.2v) the current will increase sharply due to the generation of large number of carriers at high felid run by joule heating, that induced amorphous to crystalline phase transition. This is called the threshold switching phenomena, also the resistance has been calculated too.



Figure (7):Illustrate the amorphous region and crystalline region.

This confirms that the SnSe4 is totally changed to crystalline phase. If any voltage value is applied, the I-V curve should shows a small value of resistance. Figure (7) shows that, if 2v and 4v were applied, the PCM still as crystalline, and the figure (8) shows the value of resistivity where,



Figure (8): Shows the value of resistance during crystalline phase

4.Pulse Mode test

The pulsed-mode switching behavior of PCM cell is shown in figure (9). Where this test has been done for RESET and SET states by measuring the value of resistance. A lot of different pulses of voltages have been applied. the most good pulse is 1.6v at 20 Micro second. This pulse shows that the resistor has been increased. That means the SnSe4 has been transiated from crystalline to amorphous phase.



Figure (9): Change from crystalline to amorphous after applying pulse 1.6v at 20 Microsecond

Conclusion

In summary, phase change Memory has been fabricated by using simple structure contents from (Gl, Al, SnSe4, Al). Where both Glass and Phase change material SnSe4 prepared individually and deposited by using evaporation. In this paper crystallization kinetics SnSe4 has been investigated for phase change memory applications by using annealing. The SnSe4 shows that a low threshold voltage and current can transiate from amorphous to crystalline phase the I–V measurements. in The crystallization temperature of the SnSe4 alloys are around 350 °C, which is acquired due to the phase transition and has been confirmed by X-R Diffraction results. Also band gap has been calculated by using UV test and shows that SnSe4 alloy is semiconductor from the bad gap value that was 1.65 ev. The Dc measurement shows that PCM device can transiate from amorphous to crystalline at threshold voltage of 3.2 v with high resistivity of 0.98 Mega ohm, where the crystalline resistivity is about 19.3 K ohm. Moreover, the pulse test has been investigated, where the transition process from crystalline to amorphous happened with a pulse magnitude voltage of 1.6 v and time 33 Micro second.

Recommendation for future work

This paper mainly investigated new phase change material SnSe4 alloys, where this material much cheaper than GST alloys. In further researches it is recommended to focuses on crystallite structure of SnSe4 alloys. In this paper XRD has been done but during the DC test Phase change material structure shows instability. Furthermore, Xrayphotoelectronspectroscopy(XPS)recommended. Additionally, AFM measurement (Atomic Force Microscopy) is recommended too, where this test will recognize on the nucleation rates. These suggested techniques would help in increase the efficiency. Therefore, it gives chance for further material investigation and development to make perfect Phase Change Memory devices.

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References

- [1]- B. Fulford. Unsung hero. Forbes, June 24 2002.
- [2]- iSuppli Corporation. <u>http://isuppli.com</u>.
- [3]- S. Lai. Non{volatile memory technologies: the quest for ever lower cost. In IEDM 2008, pages 01{02, 2008.
- [4]- G. E. Moore. Cramming more components onto integrated circuits. Electronics, 38(8):114{117, 1965.

- [5]- International technical roadmap for semiconductors.
 www.itrs.net/Links/2008ITRS/Update/2008 Update.pdf, 2008.
- [6]- Science X network,"Phase-change material with unexpected optical-reflectivity properties offers fresh perspectives for data storage, 2013. [Online] Available from: <u>http://phys.org/news/2013-01-phase-</u>

<u>change-material-uexpected-optical-reflectivity-</u> <u>properties.html#jCp</u> [7]- S. Lai, B Current status of the phase change

- [7]- S. Lai, B Current status of the phase change memory and its future,[in Proc. IEEE Int. Electron Devices Meeting, 2003, pp. 10.1.1– 10.1.4.
- [8]- International Technology Roadmap for Semiconductors (ITRS), 2009. [Online]. Available: http://public.itrs/net