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Control and Modification of Two Vector αβ for 48-Pulse DVR to Reduce Total Harmonic Distortion With Using Active Filter

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Keywords:
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voltage sags.

ABSTRACT

In this paper the proposed dynamic voltage restorer (DVR) can compensate the voltage unbalanced and mitigate total harmonic distortion(THD) by using active power filter (APF) during the sag condition. The suggested control algorithm employs the two vector αβ control with phase locked loop (PLL), synchronous reference frame(*dq*) and stationary reference frame (αβ) to improve the DVR performances. It extracts the fundamental components of the measured voltage and current using a 48-switch inverter connected in parallel to improve the time response and pulses. The proposed control method is tested on an 11 kV distribution system. Simulation results are obtained using PSCAD/EMITD to verify the effectiveness of the proposed control algorithm. The proposed controller with active filter can reduce the total harmonic distortion from 5% to 0.01% within 1.5 ms response for sudden sag.

التحكم وتعديل متجهين باستخدام βα ل48 نبضه في مستعيد الجهد الديناميكى لتقليل التشوه الكلى للتو افقيات باستخدام المرشح الفعال

على عمر المثنانى[1] و على ليسيود [2] و الوليد الزروق الشريف[1] و جمال العكشى[1]

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الكلمات المفتاحية:
αβ
المتحكم الطوري الحلقي المغلق (PLL)
48 نبضة لمستعيد الجهد الديناميكي
المتحكم بالاتجاهين
المتحكم مرشح القدره الفعال (APF)
الجهد الهابط .

الملخص

فى هده الورقه، مستعيد الجهد الديناميكى(DVR) يستطيع تعويض الجهد الفاقد ويقلل التشوه الكلى للتوافقيات باستخدام مرشح القدره الفعال اثناء هبوط الفولتيه. خوارزميه التحكم المقترحه تستخدم متجهين (αβ) مع متتبع الطور الحلقى المغلق (PLL) والتزامن المرجعى (*dq*) للتحسين ادا مستعيد الجهد الديناميكى . ثم استخلاص المكونات الاساسيه للتيار والجهد المقاس باستخدام عاكس به 48 مفتاح وصل بالتوازى لتحسين استجابه الزمن والنبظا ت. طريقه التحكم المقترح اختبرت على 11كيلوفولت فى نظام التوزيع. نتائج المحاكاه ثم الحصول عليها باستخدام PSCAD/EMTD لتاكيد ثاتبر خوارزميه التحكم المقترحه. المتحكم المقترح مع المرشح الفعال يستطيع تقليل التشوه الكلى للتوافقبات من% 5 الى % 0.01 خلال استجابه 1.5 ملى ثانيه للهبوط المفاجى.

I. Introduction

THD has become a problem to sensitive loads. The effect of harmonic distortion on power system operation is documented in [1]. Thus, to guarantee the operation of such loads, these harmonics should be filtered out from the supplied voltage. The traditional

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response to mitigate harmonics is the use of passive filters. Dependence on the source impedance, resonance between the passive filter and the source impedance; not being able to adapt to the changes of the load conditions. the shortcomings of the passive filter, the active filter have been proposed in [2]. Instead of providing impedance paths to current/voltage harmonics, active filters inject the same magnitude of the harmonic current/voltage.

To improve the load voltage at the desired voltage and filter out harmonics, the fundamental voltage component and the harmonic distortion of the grid voltage should be accurately detected. Hence, any employed control algorithm should perform the following tasks satisfactorily:

• separate the fundamental voltage of the grid voltage;

• estimate the harmonic voltage that should be injected. To satisfy those requirements, the new work proposes a two vector αβ control with PLL and synchronous reference frame(*dq*) to improve the DVR. DVR has been used to improve power quality against the voltage sag , swell and to extend the capability of the DVR to compensate for grid harmonics by selective harmonic control in steady-state operation. Voltage sags is commonly defined as any low voltage drop events between 10% and 90% of the nominal RMS voltage, lasting between half cycles and one min. Voltage swell, is defined as a sudden increasing of supply voltage up 110% to 180% [3]. Choi et al. in [4] introduced a kind of DVR with minimum power injection to compensate voltage disturbances on distribution system. The objective of this paper is to Modification of Two αβ- Vector Control in DVR to Reduce THD. The proposed model of the DVR considered the use of 48-switche connected parallel to improve the power to the load. The modelling and simulation of the DVR has been carried out using the electromagnetic transient simulation program PSCAD/EMTDC. Good result has obtained comparing to the previous work.

II. BASIC CONFIGURATION OF DVR

The DVR is able to compensate the voltage sag at sensitive load by injecting an appropriate voltage through an injection [5]. The DVR consists of storage unit, switching voltage source inverter (VSI), AC harmonic filter and injection transformer as shown in Fig.1.

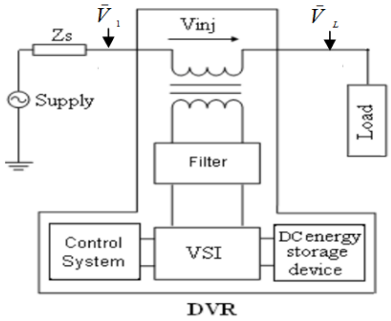

Fig.1: Basic structure of the DVR

$\bar{V}_1$, $\bar{V}_L$ and $\bar{V}_{DVR}$ are the fault supply voltage vector, the restored load voltage vector, and the DVR injection voltage vector, respectively. The DVR injection voltage can be obtained as

$$\bar{V}_{DVR} = \bar{V}_L - \bar{V}_1 \qquad (1)$$

where $\bar{V}_L$ is pre-fault load voltage vector

The DVR injects three single-phase voltages in series with the load voltage by synchronizing with the incoming supply voltage. The phase angle and magnitude of the injected voltage varies as a result of variable real and reactive power exchange between the DVR and the distribution system. The amount of real and reactive power supplied by the DVR depends on the type of voltage disturbance.

III. THD

THD is the periodic deviation of the voltage/current from the ideal sinusoidal waveform. Harmonics are sinusoidal voltage /currents, which have frequencies of multiple integer of the fundamental frequency. Harmonic current is a one of the major power quality problem to sensitive loads. The harmonic currents generated by non-linear loads will produce voltage distortion and can cause mis-operation of protection devices. Thus to guarantee the operation of such loads, these harmonics should be filtered out from the supplied voltage. To mitigate the harmonics, the passive filters is used. Passive filters provide either a low-impedance path or a high impedance block to harmonics. However, passive filters have some disadvantage such as: slow dynamic response; not being able to adapt to the changes of the load conditions. Due to the disadvantage of the passive filters, the active filters have been proposed. Active filters inject the same magnitude of the harmonic current voltage with an opposite direction to cancel the harmonics at the selected node. Ali et al. in [6] proposed passive filter for12-pulse with two vector control to reduce the THD to 0.02%. Hilmy et al in [1] proposed DVR as active filter to reduce the THD but the design will increase the power losses. Al-Matnani et al.2019 in [7] propose passive filter for 24-switche, 24-pulse DVR connected in the secondary side of transformer to reduce the leakage inductance of transformer and source harmonic. Passive filter with in phase compensation controller for 12-switche,12-pulse is design at primary side of transformer to mitigate the harmonic [8].

IV. APF

Active power filters are power electronic devices dedicated to improving the quality of the electrical energy and the efficiency of its use. The APF are circuit that use as the active device in combination with thyristor and diode to provide filter performance at low frequencies. They are operated as bistable switches, operating from non-conducting stat to conducting state. Fig. 2, shows the active filter that is connected at the output of the 48-pulse DVR to reduce and attenuate undesired frequency spectrum components that are generated from DVR. Also active filter can reduce the transient voltage that is initiated at sag start or recovery moment or caused by the nonlinear loads .

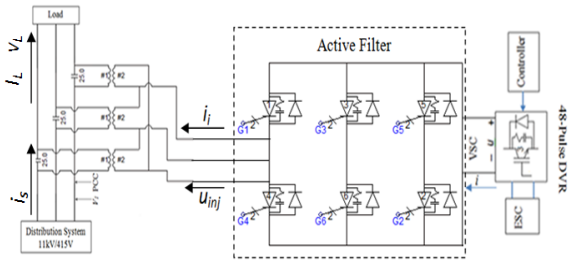

Fig. 2: Three-line diagram of DVR including, VSC, active filter and transformer

The general transfer function of active filter is,

$$\frac{U_{inj}}{u} = K_1 K_2 \frac{(S^2+\omega^2_{o1})\,(S^2+\omega^2_{o2})}{(S^2+\frac{\omega_{o1}}{Q}S+\omega^2_{o1})(S^2+\frac{\omega_{o2}}{Q}+\omega^2_{o2})} \qquad (2)$$

Where K_1, K_2 are the gains and ω_{o1} , ω_{o1} represent the frequencies. *Q* is the quality factor at different frequency.

A filter gain is the ratio of its output signal U_{inj} to its input signal *u* and is usually expressed in decibel.

Gain G_{dB} is defined as,

$$G_{dB} = 20\log\left|\frac{Uinj\ (\omega)}{u(\omega)}\right| dB \qquad (3)$$

V. TWO αβ –VECTOR CONTROL MODELING

The proposed control strategy as shown in Fig.3 is used in the DVR for injecting small active power during voltage sag, maintains constant voltage magnitude at the point under system sag, shift the inverter into the converter mode to charge the energy source capacitor(ESC) during normal state in the absence of voltage sag and force the load voltage to in-phase with the source voltage during the sag. The proposed controller is compared to the conventional controllers.

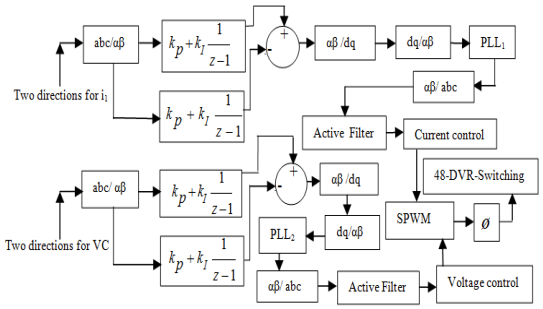

Fig. 3: Two αβ- Vector Control design

The three-phase abc to αβ transformation, filter, proportional integration (PI) controller and PLL. The PI controller is used for interpolated firing pulses and maintain the load voltage at 1 p.u. The PLL is connected between the dq/αβ and αβ/dq for tracking the system error and keep the signal in zero crossing point. The dq0 is connected between the PLL and PI controller to minimize the grid voltage error. The new controller algorithm is implemented in the dq-frame and incorporates both current and voltage controller. The Park's dqo transformation is shown as follows [9].

$$[V_d V_q V_o] = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\theta) & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta-\frac{4\pi}{3}) \\ \sin(\theta) & \sin\left(\theta-\frac{2\pi}{3}\right) & \cos(\theta-\frac{4\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (4)$$

Eq. 4 defines the transformation from a, b, c, to dqo stationary frame. Phase a is aligned to the d axis that is in quadrature with the q-axis. The θ is the angle between phase a to the d-axis.

For simplicity, zero sequence components are ignored.

$$Vo = \frac{1}{3}(Va + Vb + Vc) = 0 \quad (5)$$

$$Vd = \frac{2}{3}\left[Va\sin wt + Vb\sin\left(wt-\frac{2\pi}{3}\right) + Vc\sin\left(wt+\frac{2\pi}{3}\right)\right] \quad (6)$$

$$Vq = \frac{2}{3}\left[Va\cos wt + Vb\cos\left(wt-\frac{2\pi}{3}\right) + Vc\cos\left(wt+\frac{2}{3}\right)\right] \quad (7)$$

In this method the reference voltage for the DVR is the sine wave PWM. This is generated by comparing the pre-sag voltage with the actual voltage. The dynamic performance of the DVR may be improved by controlling the RC-filter. Two continuous vector controllers are the proportional controller to track the injected voltage and compensate the voltage loop across the RC-filter which. The injected voltage is derived as

$$V_{dvr} = V_L - V_1 \quad (8)$$

where V_L and V_1 are the load voltage and voltage at PCC.

A. Derivation of two Continuous Vector Controller

To derive the system equation as shown in Fig.2, the involved state variable include the fault supply voltage (V_1) at PCC, load voltage (V_L), series injected voltage (u_{inj})**,** active filter, current (i), series injected current(i_i) and ESC. The reference of the compensator injected voltage (u_{inj}) is obtained by subtracting the load voltage (V_L) from the nominal voltage (V_1), and then performing line to phase voltage transformation. The series injected voltage has a relation to the voltage of the voltage transformers.

To derive the controller, the APF is modelled in the stationary abc coordinates into synchronously rotating d-q. This allows the design of controllers to use DC dynamic model in balanced three-phase AC systems. As shown in Fig. 2, the state variable have null zero sequence components. Thus, d, q

The controller equation of the reference voltage and current can be derived as,

$$i^{*dq} = i_s^{dq} \pm j\frac{\omega}{2}\left\{u_{inj}^{*dq} + u_{inj}^{dq}\right\} + K_u\left\{u_{inj}^{*dq} - u_{inj}^{dq}\right\} \quad (9)$$

With respect to the PI controller, the internal gain is $Ki = \frac{K_P T_S}{T_i}$, where K_P ,T_s and T_i are the dead-beat gains, sampling time and integration time respectively. The current of the voltage source converter (VSC) is higher than the source current. This implies that if the load/source current is measured on the high voltage side, the source current i_s in Eq. (9) should be multiplied by the turns ratio of the injection transformer. The voltage drop due to the leakage impedance of the injection transformer should be calculated and added to the reference voltage of the VSC as in (10), where R_T and L_T are the resistance and leakage inductance of the injection transformer. The source voltage vector is compared against the load voltage vector. The difference between them becomes the desired injected voltage across the active filter(u_{inj}), which represents the missing voltage during the voltage sag.

$$u^{*dq} = U_{iinj}^{*dq} + R_T i_s^{*dq} \pm j\omega L_T i_s^{*dq} + i^{*dq} \pm j\frac{\omega}{2}\left\{i^{*dq} + i^{dq}\right\} + K_P\left\{i^{*dq} - i^{dq}\right\} \quad (10)$$

The present controller can control the power in two directions namely incoming direction and outgoing direction.

VI. SIMULATION RESULTS

The simulation of the proposed control strategy is carried out and the results are analysed. To illustrate the effectiveness of the active filter based DVR for voltage sag mitigation, a distribution network fed by an 11 kV voltage source is considered as shown in Fig. 2.

A. Compensating Voltage Generation

Application of DVR to voltage sag mitigation is simulated in PSCAD. Fig.4 shows the switching voltage waveforms without any transient and spike during the switching ON and switching OFF events. From the figure can be seen that the compensation voltage is generated by the DVR, that uses pulse width modulation for controlling the voltage of the DVR. The triangular waveform has a switching frequency, which is 30 times the fundamental frequency of 50 Hz, i.e. 1500 Hz. This frequency is used for switching the DVR inverter switches. The 50 Hz reference sine wave is then compared with the triangular waveform using the SPWM technique to generate the switching pulses.

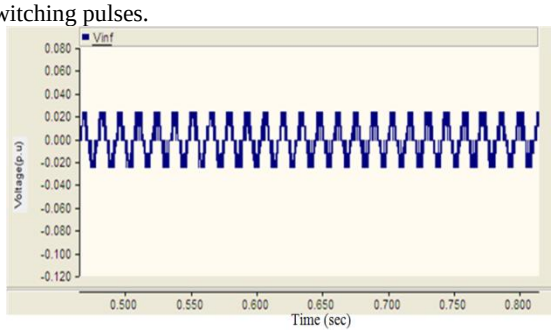

Fig.4: DVR switching voltage waveforms

B. Voltage Sag Mitigation Using DVR

The DVR is designed to compensate for voltage sag at the load side and reduce the harmonics and transient. As shown in Fig.5, the fault is chosen as a balanced three-phase fault with fault resistance and inductance of 3.033 Ω and 0.01 H respectively. From Fig.5, the fault start at time t = 0.5 sec with the duration of the fault is 0.5 sec and the percentage of sag is 22% for the voltage drops from 1.0 to 0.78 p.u. In this situation, the system needs 22% of voltage from DVR to inject into the system. Fig.6 shows the voltage injected by the DVR into the system during voltage sag. The figure shows the signal during compensation and without any voltage injected before and after the compensation.

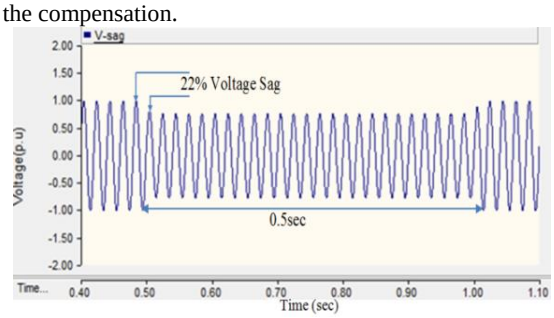

Fig.5: Voltage sag condition

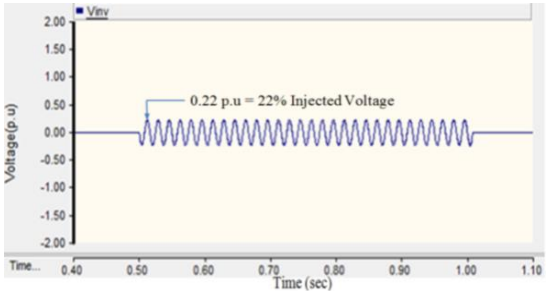

Fig.6: Voltage injected by DVR

Fig.7 shows the load voltage, which has been mitigated by DVR.

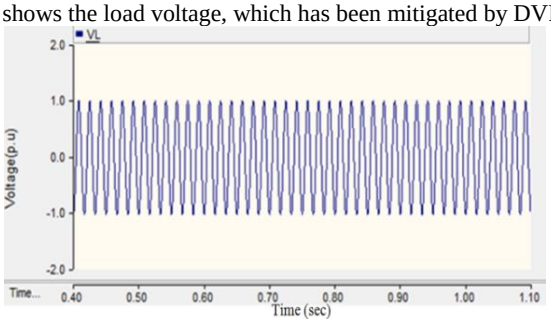

Fig.7: Load voltage

C. Harmonic Elimination in the Proposed DVR

The DVR generates the harmonic during the sag period. Because, most of the harmonic distortion is periodic. The new work can mitigate the harmonic by using active filter and Two αβ- Vector Control in DVR. Several methods can be used for reducing the harmonics produced by the DVR. Active filter is designed at the primary side of transformer to mitigate the harmonic distortion. Fig.8 and 9 shows the harmonic contents of voltage with passive filter and active filter respectively. It can be seen from Fig.9, the individual voltage harmonic contents are reduced to approximately zero when the system is connected with a active filter.

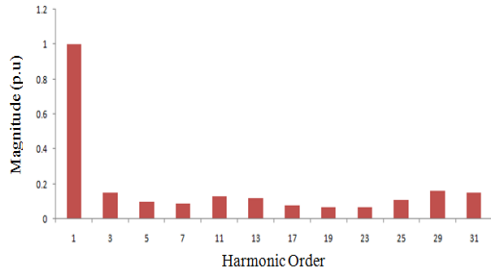

Fig.8: Voltage harmonics with passive filter

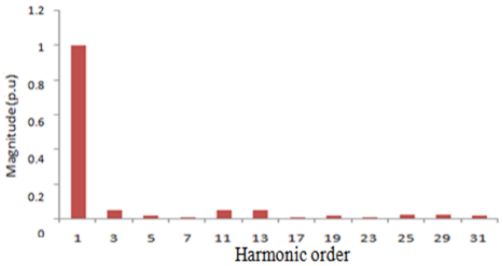

Fig.9: Voltage harmonics with active filter

Fig.10 and 11 show the THD value of the system with passive filter and with the active filter, respectively. The figures show that the THD is reduced from 5% to 0.01% with active filter that is connected at the primary of the transformer. The THD of 0.01 is far-below the value of the IEEE standard THD limit of 5%.

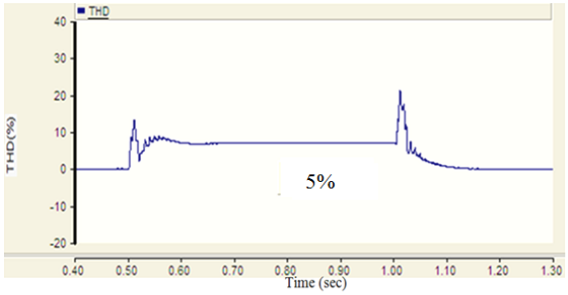

Fig.10: Total harmonic distortions for passive filter

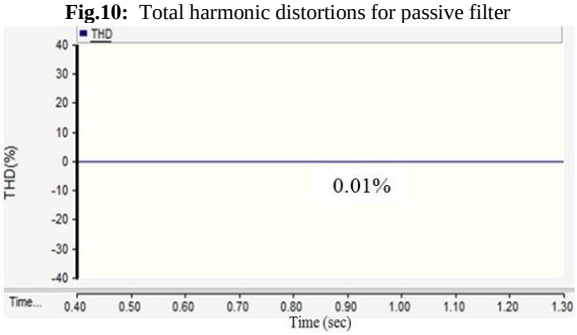

Fig.11: Total harmonic distortions for active filter

Fig 12 shows the frequency spectrum analysis for compensation voltage. Figure shows that the THD at fundamental voltage reduced to 0.01 by using active filter and αβ controller.

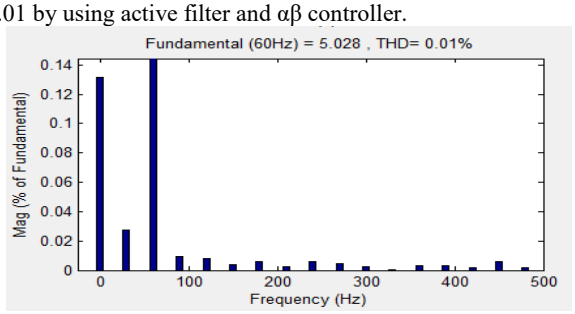

Fig.12: Frequency spectrum using active filter and αβ during compensation

If the gains of the PI controller are selected properly, the PLL will behave as a active filter. Thus, harmonics in the source voltage may not affect the performance of the PLL. The results show that the new efficient DVR can provide excellent voltage without harmonic distortion. Fig.13 shows the magnitude of the αβ-vector of the load voltage, where it is a very short time at the sag start and the sag end. This time is mainly the response time of the controller, which is 1.5ms without harmonic distortion.

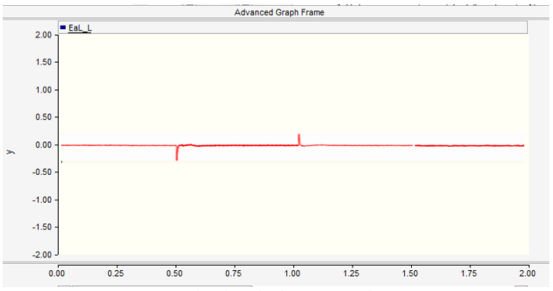

Fig.13: Magnitude of αβ-vector of load voltage

From the results shown in the previous figures, 48 switches connected in parallel with new controller and active filter can mitigate the harmonic distortion better than the same connection with passive filter as shown in Fig.14. The new work is considered to be better in performance than 48-pulse with passive filter of voltage regulation, harmonic generation and voltage sag compensation as shown in Fig.15. Figure shows the load voltage mitigated by DVR. The result show that the new design can provide excellent load voltage without harmonic distortion.

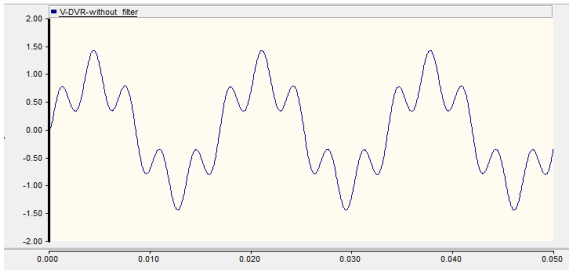

Fig.14: Harmonic distortion generated in load voltage using passive filter

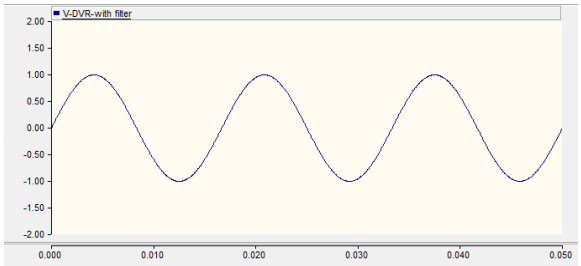

Fig.15: Load voltage without harmonic distortion using active filter

VII Conclusions

Active filter has been implemented in the Two αβ- Vector Control in DVR to Reduce THD, 5th and 7th harmonic . The DVR has been able to filter out the THD and harmonic contents of voltage and keep the THD below the required by the standards. Although, adding the filtering capability extends the function of the DVR to be as an active filter. Active filter not only reduce the effects of harmonics and high frequency spectrum but also provide power and voltage gain.

The new control strategy of the DVR demonstrates the successful result in this work. The controller can reduce the total harmonic distortion and the frequency fluctuation. The response time of the two vector αβ controller is fast and the load voltage is restored within 1.5 ms in case of unbalanced voltage sags. The dq extracted the fundamental components of the measured voltage and current. The PLL is designed to track the angle and control the frequency variation. Simulation and modelling of 48-pulse-48-switch connected in parallel to improve the voltage performance. The results showed that the proposed design and controller are better than the conventional and previous designs.

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